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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,657	08/21/2003	Naresh Maheshwari	2986P042	9938

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EXAMINER

TAT, BINH C

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/646,657

Applicant(s)

MAHESHWARI ET AL.

Examiner

Binh C. Tat

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 October 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-48 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-48 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/24/03</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 10/646657 file on 08/21/03.

Claim 1-48 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Swanson Eric.

(US Patent 67516⁹⁰~~99~~).

3. As to claims 1, 17, and 33, Swanson teaches a method to design a circuit, the method comprising: determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29); transforming a first portion of the first design to generate a second portion of a second design of the circuit (see fig fig 29-32 col 28 lines 35 to col 29 lines 59); selectively determining at least one node in the second portion of the second design (see fig fig 29-32 col 27 lines 37 to col 30 lines 54); and determining second statistical circuit activity data for the at least one node in the second portion of the second design from the first statistical circuit activity data (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29, and col 27 lines 37 to col 30 lines 54).

Art Unit: 2825

4. As to claims 2, 18, and 34, Swanson teaches wherein the first portion of the first design includes at least one of the plurality of the nodes of the first design (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29 and summary).

5. As to claims 3, 19, and 35, Swanson teaches wherein the second statistical circuit activity data comprises: a) probability information of state transition at a node (see fig 29-32 col 27 lines 37 to col 30 lines 54); b) probability information of the node being at a state (see fig 29-32 col 27 lines 37 to col 30 lines 54); and c) probability information of a group of nodes being at a state (see fig 29-32 col 27 lines 37 to col 30 lines 54).

6. As to claims 4, 20, and 36, Swanson teaches wherein a subset of nodes of the plurality of nodes of the first design remain unchanged in the second design after the first portion of the first design is transformed (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29, and col 27 lines 37 to col 30 lines 54); and, a portion of the first statistical circuit activity data is maintained for the subset of nodes in the second design (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29, and col 27 lines 37 to col 30 lines 54).

7. As to claims 5, 21, and 37, Swanson teaches further comprising: transforming a third portion of the second design to generate a fourth portion of a third design of the circuit (see fig 29-32 col 27 lines 37 to col 30 lines 54); selectively determining at least one node in the fourth portion of the third design (see fig 29-32 col 27 lines 37 to col 30 lines 54); and determining third statistical circuit activity data for the at least one node in the fourth portion of the third design from a portion of: a) the first statistical circuit activity data (see fig 29-32 col 27 lines 37 to col 30 lines 54); and b) the second statistical circuit activity data (see fig 29-32 col 27 lines 37 to col 30 lines 54).

Art Unit: 2825

8. As to claims 6, 22, and 38, Swanson teaches wherein one or more signals at the at least one node in the second portion of the second design drive the third portion of the second design (see fig 28-30 col 27 lines 23 to col 28 lines 59).

9. As to claims 7, 23, and 39, Swanson teaches wherein the second statistical circuit activity data is determined from a formal Boolean analysis (see col 1 lines 41 to col 2 lines 62).

10. As to claims 8, 24, and 40, Swanson teaches wherein the first design is one of: a) a register transfer level (RTL) design (see col 1 lines 41 to col 2 lines 62), and b) a behavioral level design (see col 1 lines 41 to col 2 lines 62); and, the first portion of the first design is transformed to generate a gate level design (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29).

11. As to claims 9, 25, and 41, Swanson teaches further comprising: selectively determining the plurality of nodes of the first design n(see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29).

12. As to claims 10, 26, and 42, Swanson teaches wherein the first statistical circuit activity data is obtained from a statistical analysis based on the first design (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29).

13. As to claims 11, 27, and 43, Swanson teaches wherein the statistical analysis comprises one of: a) a simulation based on a set of test vectors (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29 and summary); b) a simulation based on random input (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29 and summary); c) a formal analysis based on a specification of statistical input data (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29).

Art Unit: 2825

14. As to claims 12, 28, and 44, Swanson teaches wherein the plurality of nodes comprise at least one of: a) a register (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29); b) a finite state machine (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29); d) a random access memory (RAM) (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29); e) a set of registers with state constraints (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29); and f) a persistent node (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29).

15. As to claims 13, 29, and 45, Swanson teaches further comprising: determining state correlation information among the plurality of nodes of the first design; wherein the second statistical circuit activity data is further determined from the state correlation information (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29 and summary).

16. As to claims 14, 30, and 46, Swanson teaches wherein said transforming comprises one of: a) replicating a register (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29 and summary); b) pushing a register through a logic element (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29 and summary); c) changing encoding of a finite state machine (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29 and summary); d) retiming; and e) changing encoding of a group of nodes (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29 and summary).

17. As to claims 15, 31, and 47, Swanson teaches wherein at least one node in the second portion of the second design comprises a register of the second portion of the second design (see fig 29-32 col 27 lines 37 to col 30 lines 54).

18. As to claims 16, 32, and 48, Swanson teaches further comprising: determining state correlation information among the at least one node in the second portion of the second design

Art Unit: 2825

and a subset of nodes of the plurality of nodes of the first design that remain unchanged in the second design after the first portion of the first design is transformed (see fig 21-23, and 29-32 col 21 lines 43 to col 22 lines 29, and col 27 lines 37 to col 30 lines 54).

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
December 23, 2005

Thuan Do
THUAN DO
Primary examiner
12/27/05